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P.O. BOX 506, Merrifield, VA 22116, U.S.A.

TEL:+886-2-8923-7350

FAX: 806-498-6673

e-mail:winstonhsu@naipo.com

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FROM: Winston Hsu, PATENT AGENT, REG. NO.: 41,526

SERIAL NO.: 09/682,303

ATTORNEY DOCKET NO.: NAUP0303USA

SUBJECT: INFORMATION DISCLOSURE STATEMENT

TOTAL PAGES: 22 PAGES (INCLUDING COVER PAGE)

Winston Hsu 2004/10/22

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Subject: Re-submission of a previous submitted fax

Dear Sir or Madam,

This fax is a re-submission of a previous submitted fax which was sent to the above identified fax number at _02;16 AM. 10/21/2004 In the previous submission process, the fax machine failed to automatically generate a fax confirmation report. The undersigned agent has no idea whether the previous submission is completed or not. In order to avoid abandonment or delay of the correspondent U.S. patent application, the undersigned agent decides to resend this fax. If you find out that the previous fax submission is completed and the current fax becomes a redundant copy of the previous submitted fax, you can ignore this fax and use the previous fax as the formal response. Thank you very much for your help.

NAUP0303USA0_D1_1

PTC/SB/97 (09-04)

Approved for use through 07/31/2009, OMB 0651-0031

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This collection of Information is required by 37 CFR 1.8. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1.8 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the Individual case. Any comments on the amount of time you require to complete that form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450, DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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PTO/SB/08A (08-03)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary) of 1

Sheet 1

First Named Inventor Jui-Lung Chen Art Unit 2816 LUU, AN T **Examiner Name** Attorney Docket Number NAUP0303USA

			U. S. PATENT D			
Examiner Initials*	Cite No.1	Document Number	Publication Date MM-DD-YYYY	Name of Patentes or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
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FOREIGN PATENT DOCUMENTS								
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Signature Considered

*SEXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through distation if not in conformance and not considered. Include copy of this form with next communication to applicant. *Applicant's unique citation designation number (optional). *See Kinds Codes of USPTO Patent Documents at www.uspto.gog or MPEP 901.04. *Better Office that issued the document, by the two-letter code (WIPO Standard ST.3). *For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. *Kind of document by the appropriate symbols as inclosed on the document under WIPO Standard ST.16 if possible. *Applicant is to place a check mark here if English language Translation is attached.

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:

Jui-Lung Chen

Shih-Huang Huang

5 Examiner:

An T. Luu

Filing Date:

08/16/2001

Art Unit:

2816

App. No.:

09/682,303

Docket No.:

NAUP0303USA

Title:

DELAY LOCK CIRCUIT USING BISECTION ALGORITHM AND

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RELATED METHOD

To: Commissioner of Patents

P.O. Box 1450

Alexandria, VA 22313-1450

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Subject: Information disclosure statement Under

37C.F.R.\$1.56 and 37C.F.R.\$1.97(d).

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Dear Sir or Madame:

This is an Information Disclosure Statement in accordance with the duty to disclose information material to patentability under 37 C.F.R. \$1.56. Applicants wish to make of record the document listed on the accompanying form PTO/SB/08. It is respectfully requested that the Examiner initial the cited references on the form and that it be made of record in the application and that a copy of the initialed form be sent to Applicants with the next communication from the Examiner.

Since the IDS is filed after the mailing date of a notice of allowance, and on or before a payment of the issue fee, the requirement set forth in \$1.97(d) is satisfied. Items of information contained in the information disclosure statement were cited in communication from PRC Patent Office on 07/25/2004 for a counterpart foreign application.

The cited reference, JP publication number No. H10-13219, teaches a DLL circuit. As shown in Fig.1, the block diagram discloses a configuration of the cited art DLL circuit 10 14. The DLL circuit 14 comprises a phase detector 11 for comparing the phase difference between the external clock signal 6 and the internal clock signal 7, a control signal generating circuit 13 for generating a control signal 15 according to the comparison results 8-1, 8-2, 9-1, 9-2, and 10 of the phase detector 11, a plurality of delay units 3 for delaying the external clock signal 6, a multiplexer 4 for selecting a certain number of the delay units 3 according to the control signal outputted from the control signal 20 generating circuit 13, and a clock driver 5 for generating the internal clock signal 7 according to the selected delay units. A delay unit 3 is a smallest unit, which delays the external clock signal 6. Since the control signal generating circuit 13 is capable of determining a total number of used delay unit 3 according to a comparison result generated from 25 the phase detector 11, it transmits the control signal to the multiplexer 4 for driving the multiplexer 4 to select the required delay units 3.

Independent Claim 11 of the present invention, listed in the response to the Office action dated 06/03/2004, is repeated here for reference.

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- 11. A delay lock circuit for generating a second clock according to a first clock and synchronizing the first clock and the second clock, the delay lock circuit comprising:
 - a comparator for determining if corresponding periods of the first clock and the second clock are synchronized and generating a corresponding comparison signal;
 - a delayer electrically connected to the comparator for delaying the first clock so as to change a delay time between the corresponding periods of the first clock and the second clock; and

a controller to control the delay lock circuit; wherein the controller uses the delayer to perform a correcting process to increase or decrease the delay time between the corresponding periods of the first clock and the second clock by a correction interval, wherein a subsequent correction interval of a subsequent correcting process is less than a previous correction interval of a previous correcting process, and the controller terminates the correcting process if the correction interval is smaller than a predetermined value.

that "a subsequent correction interval of a subsequent correcting process is less than a previous correction interval of a previous correction process." Based on the above difference, it is believed that claim 11 is substantially different from the cited reference. And claims 12-14 are dependent on claim 11, they are believed to be substantially different from the cited reference.

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Independent Claim 16 of the present invention, listed in the response to the Office action dated 06/03/2004, is repeated here for reference.

5 16. A method for performing a delay lock to generate a second clock according to a first clock and to synchronize the second clock with the first clock, the method comprising: executing a plurality of correcting processes, each of which increases or decreases by a respective correction interval a respective delay time between corresponding periods of the first clock and the second clock; and

terminating the plurality of correcting processes when the correction interval is smaller than a predetermined value:

wherein a subsequent correction interval for a subsequent correcting process is less than a previous correction interval of a previous correcting process.

Similarly, as mentioned above, the cited reference fails to teach or suggest that "a subsequent correction interval of a subsequent correcting process is less than a previous correction interval of a previous correcting process." Based on the above difference, it is believed that claim 16 is substantially different from the cited reference. And claims 17-24 are dependent on claim 16, they are believed to be substantially different from the cited reference.

Sincerely yours,

5 Winton Hars

Date: October 21, 2004

Winston Hsu, Patent Agent No. 41,526

P.O. BOX 506

Merrifield, VA 22116

U.S.A.

10 Facsimile: 806-498-6673

e-mail: winstonhsu@naipo.com

(Please contact me by e-mail if you need a telephone communication and I will return your call promptly.)